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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,429	10/27/2000	Takenobu Tani	43889-992	4792

7590 08/03/2004

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EXAMINER	
BATAILLE, PIERRE MICHE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/697,429	TANI, TAKENOBU	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *7 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,6 and 8* is/are rejected.

7)☒ Claim(s) *2 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Correspondence

1. This Office Action is taken in response to Applicant's communication filed on June 17, 2004 in response to Official rejection and Examiner's interview. Applicant's amendments and/or arguments have been considered with the results that follow.

Claims 1-6 and 8 are pending in the application under examination as claims 7 and 9. No claims have been newly added.

Response to Arguments

2. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

The examiner indicated during the interview that the rejection is to be vacated in view of applicant's arguments. A new ground of rejection is introduced in view of newly found references as noted below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 5-6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,078,548 (Jih).

With respect to claims 1 and 8, Jih teaches a microprocessor provided with a program modification function ***[(CPU capable of modifying built-in program codes thereof and method) title; abstract; Fig. 2]***, comprising: an instruction storage unit including a ROM for storing instructions composing a program to be processed ***(a read-only memory (ROM) 10 (FIG. 2) for storing program codes)*** and a modified instruction storage unit for storing a modified instruction for program modification ***(a random-access memory (RAM) 20 (FIG. 2) for storing a special instruction and modified program codes) [abstract; Fig. 2; Col. 1, Lines 56-61]***; an address translation unit ***(special instruction detecting circuit)*** for receiving an instruction address of an instruction stored in said ROM ***(special instruction detecting circuit connected to the ROM and the RAM to drive the CPU to transfer to read said modified program codes in the RAM when said special instruction is detected) [abstract; Col. 2, Lines 5-12, Lines 17-21; Col. 4, Lines 20-41]***. Jih fails to explicitly teach translating instruction address into a substitute address at which the modified instruction is stored in said modified instruction storage unit. However, Ogata discloses a system and known method modifying program in the computer system ***(Fig. 1-2)*** comprising a microcomputer and external memory, the microcomputer comprising a nonerasable ROM having stored therein a basic program and basic data for controlling the operation of the computer system, a RAM for storing various programs, a CPU for executing programs ***[Fig. 1]***, wherein the microcomputer transfers a modification program from the external memory to the RAM ***[Col. 1, Lines 49-55]*** and the microcomputer has stored therein a modifying address indicating the location where the

data contained in the basic program is to be modified and a RAM address where the data of the modification program to be substituted at the modifying address is stored ***[Col. 1, Line 63 to Col. 2, Line 3]***. Therefore it would have been obvious to one of ordinary skill in the art to translate instruction address into a substitute address, as taught by Ogata, in conjunction to the code update method of Jih, because the microcomputer would have executed the modification program when executing the portion to be modified of the basic program, as taught by Ogata ***[Col. 1, Lines 56-59]***. The modification is proper because Ogata teaches that the basic program is executed as modified when executing the portion to be modified of the basic program ***[Col. 1, Lines 56-59]***.

With respect to claim 6, Jih teaches the address translation unit is composed of a field programmable logic which outputs translated address in accordance with received instruction address ***[Col 3, Line 62 to Col. 4, Line 9]***.

With respect to claims 3 and 5, Ogata teaches occurrence of an address by k^{th} address and reference to code offset to jump to head address of k^{th} modification program code ***[Fig. 2 and Fig. 4]***; Jih additionally teaches said address translation unit outputting translated addresses in accordance with received instruction address ***[abstract; Col. 2, Lines 5-12]*** and address bit width to be a translation target is changeable when the instruction address is translated ***[abstract; Col. 2, Lines 22-29; Col. 4, Lines 21-47]***.

Allowable Subject Matter

5. Claims 2 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,790,860 (Wetmore et al) teaching method and apparatus for patching code residing on read only memory device.

"Dual Indirect RAM/ROM Jumptable for Firmware Update", IBM Technical Disclosure Bulletin, vol. 31, No. 1, Jun. 1988, pp. 294-298.

US 2002/062479 (Takata) teaching microcontroller with modifiable program.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

July 26, 2004